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Research Interests

§Theory and development of advanced DSP algorithms for performance enhancement of wideband digital receivers §Development of efficient VLSI test and testability structures for System-on-a-chip (SoC) applications §Mixed-signal design and verification of Receiver-On-a-Chip (ROC) §Low-power design of efficient fast Fourier transform (FFT) architecture §VLSI and FPGA implementation of high-performance algorithms §Biologically-inspired electronics and designs

Current Research

Wideband Digital Receivers

One of the most predominant trends in modern microwave signals is the move toward wider bandwidths. Analog wideband receiver designs can accommodate the technology-stressing bandwidths, but come at a cost of reduced flexibility. Digital approaches, on the other hand, provide flexibility in receiver signal processing, but they are limited by analog-to-digital converter resolution and power consumption. The goal of this research is to design and implement a 1-GHz signal bandwidth digital receiver which uses the Kaiser Window function and compensation technique. The Kaiser Window reduces the spectral leakage by eliminating the discontinuities at the time window edges and the compensation uncovers the weak signal for extension of the two-signal spurious free dynamic range (SFDR) of the receiver. The combination of both techniques extends the two-signal SFDR of the receiver to 24 dB. A novel hardware implementation using look-up tables for FFT, Kaiser Window and the compensation method is being developed. We are also exploring algorithms for multiple signal detection and data modulation using a configurable wideband digital receiver.

Logic Built-In Self-Test

System-on-a-chip (SoC) built with embedded IP cores offers attractive methodology design reuse, reconfigurability, and customizability. But integration of design-for-testability (DfT)

structures of IP cores in these complex SoCs presents daunting challenges to designers and ultimately affects the time-to-market goals. In this research, we are exploring a design methodology to reduce the time-to-market by taking core test data from the design environment and automatically generating DfT structures that can be easily integrated into SoC. A novel automated synthesis methodology to generate SoC built-in self-test (BIST) in order to test IP and custom logic cores with high fault coverage is proposed. The proposed technique, Non Exclusive-Xor Test of 2-D LFSR (NEXT 2-D LFSR) generates a deterministic sequence of test vectors for random-vector-resistant faults, and then random test vectors for random-vector-detectable faults. It is also capable of optimizing 2-D LFSRs with consideration of don't-care bits in incompletely specified test patterns.

FPGA implementation of SigmaRho Kalman filter

There are changes ongoing within the embedded design space where higher degrees of parallelism are being used to achieve higher throughput at lower cost. We are investigating a FPGA implementable Architecture for SigmaRho adaptation of Kalman filter. The field programmable gate array (FPGA) logic hardware devices can provide high parallelism and are now widely considered for implementation of high-performance algorithms. Some of the advantages of implementing algorithms on an FPGA are : 1) integer math is not restricted to the standard 8-, 16-, 32-bit modes as in C compilers and significant benefits can be derived from working with smaller bit widths, 2) both parallelism and pipelining are key enablers for speed. The Kalman filter allows parallelism because the equations are naturally expressed as loops. The loops can be unrolled so that the implied computations can be performed on a single instruction of the FPGA device. Pipelining is also naturally afforded by the sigmaRho mechanization. For pipelining, sequential steps of the processing are performed simultaneously, yielding results that correspond to prior sample epochs.

ASIC implementation of Ultrasound Digital Beamformer for Array Transducers

High-frequency (>20 MHz) ultrasound has demonstrated high spatial resolution on the submillimeter level, and has been successfully applied to ophthalmology, dermatology, small animal imaging, and intravascular imaging. The objective of the proposed research is to design a microchip for a 16-channel real-time high frequency digital beamformer for the digitized echoes from 16 adjacent transducer elements. Beamforming is a signal processing technique used in transducer arrays for directional signal reception. The design will have the hardware architecture that provides great flexibility for beamforming, such as dynamic focusing in transmission and reception of the ultrasound waves. The ASIC design will provide great flexibility for beamforming, such as dynamic receive focusing and receive apodization.

Education

Ph.D. Wright State University, Dayton, Ohio – 2007

Dissertation title “Design and Performance Evaluation of a 2.5-GSPS Wideband Digital Receiver”

M.S. Wright State University, Dayton, Ohio – 2002

B.S. Bharathiar University, India – 1999

Honors and Awards

2008 Recipient of Best Senior Design Project advisor: Computer Engineering

2007 Accepted into “Marquis Who's Who in America”, (2008, 62nd Anniversary Edition)

2006 Recipient of the Dean’s award for Outstanding Graduate Student (Ph. D. Engineering program)

2006 Accepted into “Marquis Who's Who in America”, (2007, 61st Anniversary Edition)

2006 Accepted into "Strathmore's Who's Who" registry for outstanding professionals (2006-2007, 13th Anniversary Edition)

2006 Accepted into "America’s registry for outstanding professionals”, (2006-2007, 11th Anniversary edition)

2006 Recipient of Ph.D. Engineering Scholarship Wright State University

2003 Recipient of Competitive DAGSI scholarship, Home institution - Wright State University

Research and Professional Experience

08/2007 – Present **Assistant Professor**, Computer Engineering, California State University, Fullerton

- Taught computer engineering courses (Microcontrollers, Advanced Electronics, Embedded processor interfacing)
- Revised existing courses and proposed new VLSI courses
- Prepared proposal for upgrading the VLSI lab
- Participated in several academic and administrative committees
- Provided capstone senior design project guidance

06/2003 – 06/2007 **Research Assistant**, Dept. of Electrical Engineering, Wright State University, Dayton, Ohio

- Designed and implemented 2.5 giga-sample per second (GSPS) receiver-on-a-chip (ROC)
- Developed automated synthesis flow for the configurable 2D

LFSR with SoC BIST applications

- Designed and evaluated data windowing structure to improve two-signal instantaneous dynamic range of wideband receivers
- Researched on noise effect on sensitivity and two-signal instantaneous dynamic range of 1-GHz wideband digital receiver
- Designed and implemented a configurable wideband digital receiver for simultaneous detection and measurement of multiple signals
- Designed and implemented a configurable look-up table FFT processor for wideband digital receivers in radar applications
- Adapted the 2-D LFSR design to take in don't-care test patterns for BIST synthesis

06/2003 – 06/2005 **Graduate Project Assistant**, Receiver-On-a-Chip (ROC) project, funded by Air Force research lab (AFRL)

- Conducted preliminary investigation into possible ADC implementations and fabrication technologies
- Developed and evaluated compensation algorithm for digital receivers
- Developed an efficient hardware for super-resolution block utilizing high-speed arithmetic structures
- Developed a mixed floating and fixed point hardware for super-resolution block using novel lookup-table (LUT) multipliers
- Estimated optimum data width in Matlab receiver simulation
- Implemented the super-resolution block in IBM 0.13 μm CMOS process

03/1999 – 02/2000 **Graduate Trainee**, Cochin Refineries, India

- Actively participated in Tank farm automation and Diesel Hydro-Desulphurisation (DHDS) Unit projects
- Underwent training in the maintenance department

Journal publications

- [1] K. George, C.-I. H. Chen, and J. B. Y. Tsui “Extension of Two Signal Dynamic Range of Wideband Digital Receivers using Kaiser Window and Compensation Method,” *IEEE Trans. Microwave Theory and Techniques*, vol. 55, no. 4, pp. 788– 794, April, 2007.
- [2] C.-I. H. Chen, K. George, W. McCormick, J. B. Y. Tsui, S. L. Hary, and K. M. Graves,

“Design and performance evaluation of a 2.5-GSPS Digital Receiver”, *IEEE Trans. Instrumentation and Measurement*, vol. 54, no. 4, pp. 1089-1099, June 2005.

- [3] C.-I. H. Chen and K. George, “Configurable two-dimensional Linear Feedback Shifter Registers for parallel and serial Built-In Self-Test”, *IEEE Trans. Instrumentation and Measurement*, vol. 53, no. 4, pp. 1005-1014, August 2004.

Conference publications

- [4] George, K. and Chen, C.-I. H., “Logic Built-In Self-Test for Core-Based Designs on System-on-a-Chip,” *Proc. IEEE International Instrumentation and Measurement Technology Conf.*, pp. 1503-1508, Vancouver, British Columbia, Canada, May 2008.
- [5] George, K. and Chen, C.-I. H., “Multiple Signal Detection and Measurement Using a Configurable Wideband Digital Receiver,” *Proc. of IEEE International Instrumentation and Measurement Technology Conf.*, Warsaw, Poland, May, 2007.
- [6] George, K. and Chen, C.-I. H., “Configurable and Expandable FFT Processor for Wideband Communications,” *Proc. of IEEE International Instrumentation and Measurement Technology Conf.*, Warsaw, Poland, May, 2007.
- [7] K. George, C.-I. H. Chen, and J. B. Y. Tsui “Extension of Two Signal Spur Free Dynamic Range of Wideband Digital Receivers using Kaiser Window and Compensation Method”, *Proc. IEEE MTT International Microwave Symposium*, pp. 1955-1958, June 2006.
- [8] C.-I. H. Chen and K. George, “2.5 GSPS/1 GHz Wide Band Digital Receiver”, *Proc. IEEE Industrial Electronics*, vol. 2, pp. 1888-1893, Nov. 2003.
- [9] C.-I. H. Chen, K. George, and J. B. Y. Tsui, “Design and measurement of 2.5 GSPS Digital Receiver”, *Proc. IEEE Instrumentation and Measurement technology Conf.*, vol. 1, pp. 258-263, May. 2003.
- [10] C.-I. H. Chen and K. George, “Configurable two-dimensional Linear Feedback Shift Registers for Built-In Self-Test”, *Proc. IEEE Instrumentation and Measurement technology Conf.*, vol. 2, pp. 1431-1436, May. 2003.
- [11] C.-I. H. Chen and K. George, “Configurable two-dimensional Linear Feedback Shift Registers for random patterns logic BIST”, *Proc. Int. Symp. Circuits and Systems*, vol. 5, pp. 25-28, May. 2003.
- [12] C.-I. H. Chen and K. George, “Automated synthesis of Configurable two-dimensional Linear Feedback Shifter Registers for random/embedded test patterns”, *Proc. Int. Symp. Quality Electronic Design*, vol. 5, pp. 24-26, March. 2003.

Reviewer of technical journals and conferences

IEEE International Symposium on Circuits and Systems

IEEE International Conference on Electronics, Circuits and Systems

IEEE Transactions on Computers

IEEE Transactions on Signal Processing

IEEE Transactions on Instrumentation and Measurement

IEEE Transactions on Circuits and Systems (I), (II)

Professional memberships

IEEE, Member

IEEE, International Microwave Society

IEEE, Instrumentation and Measurement Society